

AMENDMENTS TO THE CLAIMS

- 1.(Currently amended) A Global Positioning System(GPS) receiver, comprising:
- a Radio Frequency (RF) Front End, comprising:
- single state downconverter using dual mixers;
- an I/Q Intermediate Frequency (IF) active filter, coupled to the downconverter;
- an Automatic Gain Control (AGC) amplifier, coupled to the downconverter;
- an Analog-to-Digital Converter (ADC) coupled to the AGC amplifier; and
- a frequency synthesizer section including an integrated Voltage Controlled Oscillator and a reference oscillator with a frequency of 24.5535 MHz plus or minus 40 parts per million (ppm); and
- a digital processing section, coupled to the RF Front End, wherein the noise bandwidth of the GPS receiver is set by the IF active filter.
- 2.(Previously presented) The GPS receiver of claim 1, further comprising a Low Noise Amplifier (LNA) coupled to an RF band select filter, which is coupled to an RF input of the RF front end.
- 3.(Original) The GPS receiver of claim 1, wherein output interface signals of the RF Front End are Positive Emitter Collector Logic (PECL) compatible.

4.(Original) The GPS receiver of claim 3, wherein the PECL compatible outputs of the RF Front End further include an acquisition clock (ACQCLK) signal generated by the frequency synthesizer section.

5.(Original) The GPS receiver of claim 4, wherein the ACQCLK signal has a frequency approximately equal to $37.3333f_0$, where $f_0=1.023$ MHz.

6.(Original) The GPS receiver of claim 5, wherein the PECL compatible outputs further include a GPS clock (GPSCLK) signal output from the frequency synthesizer section.

7.(Original) The GPS receiver of claim 6, wherein the GPSCLK signal has a frequency approximately equal to $48f_0$, where $f_0=1.023$ MHz.

8-11(Canceled)

12.(Currently amended) The GPS receiver of claim 1 wherein the frequency synthesizer section comprises:

~~a reference oscillator;~~

a frequency doubler coupled to the reference oscillator;

a divide-by-9 circuit coupled to the frequency doubler;

a phase and frequency detector (PFD) coupled to the divide-by-9 circuit;

a charge pump coupled to the PFD;

and the voltage controller oscillator (VCO) that is also coupled to the downconverter;

a divide-by-41 circuit coupled to the VCO; and

a divide-by-7 circuit coupled between the divide-by-41 circuit and the PFD to make a phase locked loop.

13.(Previously presented). The GPS receiver of claim 12 wherein the reference oscillator is adapted for receiving an external reference signal.

14. (Previously presented). The GPS receiver of claim 12 further comprising a crystal for providing an external reference signal to the reference oscillator.

15. (Previously presented). The GPS receiver of claim 1, comprising an external antenna assembly.

16. (Previously presented). The GPS receiver of claim 15, wherein the external antenna assembly comprises an antenna, and LNA, and an RF bandpass filter.

17. (Previously presented). The GPS receiver of claim 1 wherein the RF Front End comprises an external loop filter.

18. (Previously presented). The GPS receiver of claim 1 comprising an I/Q combiner circuit coupled to the IF active filter for combining filtered I-IF and Q-IF outputs received therefrom and outputting a single IF output signal to the AGC amplifier.

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